L Number	Hits	Search Text	DB	Time stamp
1	111352	(leaf or module or tils or bitcell) same (block or decoder or array)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:02
2	1373	hierarchical$4 near8 (stitch$4 or arrange or interconnect$5)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:03
3	302	((leaf or module or tils or bitcell) same (block or decoder or array)) and (hierarchical$4 near8 (stitch$4 or arrange or interconnect$5))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:03
4	8	(((leaf or module or tils or bitcell) same (block or decoder or array)) and (hierarchical$4 near8 (stitch$4 or arrange or interconnect$5))) and parametric	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:03
5	2	(((leaf or module or tils or bitcell) same (block or decoder or array)) and (hierarchical$4 near8 (stitch$4 or arrange or interconnect$5))) and dataset	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:04
6	79	(((leaf or module or tils or bitcell) same (block or decoder or array)) and (hierarchical$4 near8 (stitch$4 or arrange or interconnect$5))) and data and horizontal and vertical	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:04
7	35	((((leaf or module or tils or bitcell) same (block or decoder or array)) and (hierarchical$4 near8 (stitch$4 or arrange or interconnect$5))) and data and horizontal and vertical) and netlist	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:04
8	32	(((((leaf or module or tils or bitcell) same (block or decoder or array)) and (hierarchical$4 near8 (stitch$4 or arrange or interconnect$5))) and data and horizontal and vertical) and netlist) and simulat$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:09
9	13557	(bitcell or (flip adj flop) or (storage adj element) or register) near4 array	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:11
10	33	((bitcell or (flip adj flop) or (storage adj element) or register) near4 array) and ((leaf or module or tils or bitcell) same (block or decoder or array)) and (hierarchical$4 near8 (stitch$4 or arrange or interconnect$5))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:15
11	33	((bitcell or (flip adj flop) or (storage adj element) or register) near4 array) and (((leaf or module or tils or bitcell) same (block or decoder or array)) and (hierarchical$4 near8 (stitch$4 or arrange or interconnect$5)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:15
12	4	((bitcell or (flip adj flop) or (storage adj element) or register) near4 array) and ((((leaf or module or tils or bitcell) same (block or decoder or array)) and (hierarchical$4 near8 (stitch$4 or arrange or interconnect$5))) and parametric)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:15

13	31	(((bitcell or (flip adj flop) or (storage adj element) or register) near4 array) and (((leaf or module or tils or bitcell) same (block or decoder or array)) and (hierarchical$4 near8 (stitch$4 or arrange or interconnect$5)))) and (input/output or I/O)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:16
14	12	((((bitcell or (flip adj flop) or (storage adj element) or register) near4 array) and (((leaf or module or tils or bitcell) same (block or decoder or array)) and (hierarchical$4 near8 (stitch$4 or arrange or interconnect$5)))) and (input/output or I/O)) and netlist	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:16
15	12	(((((bitcell or (flip adj flop) or (storage adj element) or register) near4 array) and (((leaf or module or tils or bitcell) same (block or decoder or array)) and (hierarchical$4 near8 (stitch$4 or arrange or interconnect$5)))) and (input/output or I/O)) and netlist) and simulat$4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/07 18:16

	Document ID	Issue Date	Pages	Title	Current OR
1	US 20040004496 A1	20040108	18	Field programmable gate array with convertibility to application specific integrated circuit	326/39
2	US 6546532 B1	20030408	31	Method and apparatus for traversing and placing cells using a placement tool	716/8
3	US 6407434 B1	20020618	136	Hexagonal architecture	257/401
4	US 6363516 B1	20020326	14	Method for hierarchical parasitic extraction of a CMOS design	716/5
5	US 6324678 B1	20011127	45	Method and system for creating and validating low level description of electronic design	716/18
6	US 6312980 B1	20011106	134	Programmable triangular shaped device having variable gain	438/197
7	US 6216252 B1	20010410	53	Method and system for creating, validating, and scaling structural description of electronic device	716/1
8	US 6195788 B1	20010227	21	Mapping heterogeneous logic elements in a programmable logic device	716/18

	Document ID	Issue Date	Pages	Title	Current OR
9	US 6097073 A	20000801	138	Triangular semiconductor or gate	257/401
10	US 5973376 A	19991026	136	Architecture having diamond shaped or parallelogram shaped cells	257/401
11	US 5889329 A	19990330	139	Tri-directional interconnect architecture for SRAM	257/758
12	US 5872380 A	19990216	136	Hexagonal sense cell architecture	257/369
13	US 5870308 A	19990209	49	Method and system for creating and validating low-level description of electronic design	716/18

	Document ID	Issue Date	Pages	Title	Current OR
14	US 5864165 A	19990126	141	Triangular semiconductor NAND gate	257/401
15	US 5834821 A	19981110	140	Triangular semiconductor "AND" gate device	257/401
16	US 5822214 A	19981013	135	CAD for hexagonal architecture	716/10
17	US 5811863 A	19980922	136	Transistors having dynamically adjustable characteristics	257/401

	Document ID	Issue Date	Pages	Title	Current OR
18	US 5808330 A	19980915	136	Polydirectional non-orthoginal three layer interconnect architecture	257/208
19	US 5801958 A	19980901	95	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information	716/18
20	US 5801422 A	19980901	139	Hexagonal SRAM architecture	257/369
21	US 5789770 A	19980804	136	Hexagonal architecture with triangular shaped cells	257/206

	Document ID	Issue Date	Pages	Title	Current OR
22	US 5777360 A	19980707	137	Hexagonal field programmable gate array architecture	257/315
23	US 5742181 A	19980421	16	FPGA with hierarchical interconnect structure and hyperlinks	326/41
24	US 5742086 A	19980421	136	Hexagonal DRAM array	257/300
25	US 5696693 A	19971209	47	Method for placing logic functions and cells in a logic design using floor planning by analogy	716/8
26	US 5598344 A	19970128	51	Method and system for creating, validating, and scaling structural description of electronic device	716/18
27	US 5572436 A	19961105	48	Method and system for creating and validating low level description of electronic design	716/18
28	US 5557531 A	19960917	47	Method and system for creating and validating low level structural description of electronic design from higher level, behavior-oriented description, including estimating power dissipation of physical implementation	716/1

	Document ID	Issue Date	Pages	Title	Current OR
29	US 5555201 A	19960910	95	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information	716/1
30	US 5553002 A	19960903	47	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, using milestone matrix incorporated into user-interface	716/11
31	US 5544066 A	19960806	47	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including estimation and comparison of low-level design constraints	716/18
32	US 5541849 A	19960730	46	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including estimation and comparison of timing parameters	716/18